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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Huilong ZHU	Group Art Unit: 2818
Appln. No.	:	10/707,840	Examiner: Nguyen, Dao H.
Filed	:	January 16, 2004	Confirmation No: 1839
For	:	PROTECTING SILICON GERMANIUM SIDEWALL WITH SILICON FOR STRAINED SILICON/SILICON GERMANIUM MOSFETS	

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action dated October 12, 2005, please amend the above-identified application as follows.

Amendments to the Specification begin on page 2.

A listing of claims is set forth on pages 4.

Remarks are set forth on pages 8.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. 09-0458.

AMENDMENT TO SPECIFICATION

IN THE SPECIFICATION:

A marked-up copy of the changes to selected paragraph(s) is provided below. Please enter these changes to the specification in the record.

Please replace paragraph [0017] with the following paragraph:

[0017] Referring to FIG. 1, an exemplary initial structure employed in the invention is shown. Specifically, the exemplary initial structure is comprised of an SOI substrate 105 having a patterned gate stack region 110 formed on the surface thereof. The SOI substrate 105 may include a buried oxide layer ~~125~~ 135 sandwiched between a top Si-containing layer 130 and a bottom Si-containing layer 140. The top Si-containing layer 130 is an area upon which devices may be formed. The Si-containing layer 130 may be comprised of various semiconducting materials that include silicon, such as Si, SiGe, SiC, SiGeC, Si/Si, or Si/SiGe.

Please replace paragraph [0025] with the following paragraph:

[0025] Silicon layers 155 and 170 may be formed on the SiGe layers 150 and 165 of the raised source and drain regions 160 and 175, respectively, using a conventional selective epitaxial silicon formation technique. For example, molecular beam epitaxy (MBE) may be used to selectively grow device quality silicon. Because Si has a smaller lattice constant (i.e., atom spacing) than Ge, when Si 155 and 170 is grown on the SiGe layer 160 and 165, the Si 155 and 170 is strained in tension. A suitable thickness for the strained Si layers 155 and 170 is below the critical thickness, which is the maximum thickness that strained Si can grow on the ~~SiGe~~ SiGe layers 150 and 165 without forming defects in the crystal structure (e.g., dislocations). By way of example but not limitation, the strained Si layer 155 may be approximately 5 to 100 nm thick.

Please replace paragraph [0031] with the following paragraph:

[0031] The spacers 505 and 525 may be formed along the Si coated SiGe sidewalls of the raised drain in a conventional manner, such as by oxide deposition, patterning and etching using processes known in the art. After formation of the spacers, an additional selective epitaxial growth step may be performed to complete formation of the raised drain. The oxide spacers 505 and 525 will prevent further formation of Si along the sidewalls during the additional selective epitaxial growth step. After completing the ~~sadditional~~ additional selective epitaxial growth step, the oxide spacers may be removed, such as by dry etching.

AMENDMENT TO THE CLAIMS

Please **AMEND** claims 1 and 13 as follows.

Please **CANCEL** claims 12 and 23-28.

Please **ADD** claims 29-34 as follows.

A copy of all pending claims and a status of the claims is provided below.

Claim 1. (currently amended) A method of fabricating a semiconductor structure, comprising the steps of:

forming a raised source region on a substrate;

forming a raised drain region on the substrate; and

forming a first silicon layer over the raised source region and a second silicon layer over the raised drain region,

wherein the first silicon layer formed over the raised source region and the second silicon layer over the raised drain region include cap portions and sidewall portions, the method further comprising a step of forming sacrificial spacers along the silicon sidewall portions.

Claim 2. (original) A method according to claim 1, wherein the substrate includes a SiGe layer atop a buried oxide layer.

Claim 3. (original) A method according to claim 1, further comprising a step of forming a gate stack on the substrate.

Claim 4. (original) A method according to claim 3, further comprising a step of forming a trench isolation surrounding the gate stack, source region and drain region.

Claim 5. (original) A method according to claim 1, further comprising a step of forming a first silicide contact on the first silicon layer.

Claim 6. (original) A method according to claim 1, further comprising a step of forming a second silicide contact on the second silicon layer.

Claim 7. (original) A method according to claim 1, wherein the first silicon layer is epitaxially formed silicon and the second silicon layer is epitaxially grown silicon.

Claim 8. (original) A method according to claim 1, wherein the raised drain region is comprised of a strained silicon layer atop a SiGe layer.

Claim 9. (original) A method according to claim 8, wherein the strained silicon layer is comprised of epitaxially grown silicon.

Claim 10. (original) A method according to claim 1, wherein the raised source region is comprised of a strained silicon layer atop a SiGe layer.

Claim 11. (original) A method according to claim 10, wherein the strained silicon layer is comprised of epitaxially grown silicon.

Claim 12. (canceled)

Claim 13. (currently amended) A method according to claim ~~12~~ 1, further comprising steps of:

forming a third silicon layer over the cap of the first silicon layer over the raised source region; and

forming a fourth silicon layer over the cap of the second silicon layer over the raised drain region.

Claim 14. (original) A method according to claim 13, further comprising a step of removing the sacrificial spacers.

Claim 15. (original) A method according to claim 14, wherein the step of removing the sacrificial spacers includes etching away the sacrificial spacers.

Claims 16-28 (cancelled)

Claim 29. (new) A method of fabricating a semiconductor structure, comprising:

forming a raised source region on a substrate;

forming a raised drain region on the substrate;

forming a strained silicon layer on the raised source region and the raised drain region; and

forming a silicon cap on the strained silicon layer.

Claim 30. (new) A method according to claim 29, further comprising forming silicon sidewalls on the raised source region and the raised drain region.

Claim 31. (new) A method according to claim 30, further comprising forming sacrificial spacers along the silicon sidewalls.

Claim 32. (new) A method according to claim 31, further comprising forming a silicon layer on the silicon cap.

Claim 33. (new) A method according to claim 32, further comprising removing the sacrificial spacers.

Claim 34. (new) A method according to claim 33, further comprising forming silicide contacts on the silicon layer.

REMARKS

Claims 1-11, 13-15, and 29-34 are currently pending in the application. By this amendment, claims 1 and 13 are amended and claims 29-34 are added for the Examiner's consideration. Claims 12 and 23-28 are canceled. The above amendments do not add new matter to the application and are fully supported by the specification. For example, support for the amendments is provided at Figures 4-5 and at paragraphs 0029-0032 of the specification. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Objection to Claims

Claims 12 was objected to for a typographical error. By this amendment, claim 12 has been canceled. Accordingly, the objection to the claim should be withdrawn.

Claims 23-28 were objected to for phrases in the preamble and for repeating limitations. By this amendment, claims 23-28 have been canceled. Applicants reserve the right to file these claims in a continuing application. Accordingly, the objection to the claims should be withdrawn.

35 U.S.C. §102 Rejection

Claims 1-4 and 7 were rejected under 35 U.S.C. §102(b) for being anticipated by U. S. Patent No. 6,420,766 issued to Brown *et al.* ("Brown"). Claims 1, 5-6, 8-15, and 23-28 were rejected under 35 U.S.C. §102(b) for being anticipated by U. S. Patent No. 6,214,679 issued to Murthy *et al.* ("Murthy"). These rejections are respectfully traversed.

To anticipate a claim, each and every element as set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. MPEP §2131. Applicants submit that the references supplied by the Examiner do not show each and every feature of the claimed invention.

The instant invention generally relates to a semiconductor device and method of manufacture and, more particularly, to a semiconductor device that includes strained

silicon/silicon germanium field effect transistors with a protective silicon layer. Claim 1, which includes the features of original claim 12, recites in pertinent part:

> ...forming a first silicon layer over the raised source region and a second silicon layer over the raised drain region;
>
> wherein the first silicon layer formed over the raised source region and the second silicon layer over the raised drain region include cap portions and sidewall portions, the method further comprising a step of forming sacrificial spacers along the silicon sidewall portions.

Neither Brown nor Murthy shows these features, and therefore neither anticipates the claim.

Brown

Brown shows a semiconductor comprising a substrate 2500, raised source 2806, and raised drain 2808. Brown also shows a first silicon layer 3502 and a second silicon layer 3502 formed over the raised source and drain. However, Brown does not include a cap portion or sidewall portions, or the step of forming sacrificial spacers along the sidewall portions. The Examiner implicitly agrees with this since, in the Office Action, there was no assertion that Brown anticipated claim 12. Therefore, Brown does not contain each and every element of claim 1 and does not anticipate claims 1-4 and 7.

Murthy

The Examiner is of the opinion that Murthy shows the features of the claimed invention. The Examiner points to figure 9 and columns 3-8 as disclosing the step of forming silicon layers over the raised source and drain. The Examiner asserts that element 234 is a cap portion and element 232 is a sacrificial spacer along silicon sidewall portions. Applicants respectfully disagree.

Applicants submit that Murthy shows raised source and drain regions without any protective silicon layer. For example, Murthy shows forming raised source and drain regions 218 on a substrate (fig. 6). Murthy shows subsequently applying an oxide layer

to the raised source and drain, and a silicon-nitride layer over the oxide layer (fig. 7). Murthy then teaches selectively removing the oxide and silicon-nitride layers from the source and drain (fig. 8) and performing a high energy deep source/drain implant into the substrate (fig. 9; lines 15-26 of col. 7). Cobalt film 232 is deposited over the source and drain, and a titanium nitride layer 234 is deposited over the cobalt film (fig. 10). The device is heated such that the cobalt film 232 reacts with the source/drain 218 to form a monocobaltgermanosilicide film 236 over the source/drain (fig. 11). Any unreacted cobalt and titanium nitride is then removed (fig. 12).

Contrary to the Examiner's assertion, the implantation step shown in figure 9 and discussed in column 7 does not result in a silicon layer being formed over the source and drain regions as recited in the claimed invention. It is clearly seen in figure 9 that this step does not result in the formation of any layer over the source/drain region . And Murthy makes no mention whatsoever of the formation of a silicon layer during the discussion of this ion-implantation step. Further contrary to the Examiner's assertion, element 234 is in fact a titanium-nitride layer, and is not a cap portion of a silicon layer formed over the source/drain region. Even further, Murthy does not disclose, and the Examiner does not identify any element as, a sidewall portion of a silicon layer formed over the source/drain region. Even further, since there is no silicon sidewall portion, cobalt film 232 does not constitute a sacrificial spacer *along a silicon sidewall portion* as recited in the claimed invention. The above-noted claimed features simply are not present in Murthy. Therefore, Murthy does not disclose the elements of claim 1 and does not anticipate claims 1, 5-6, 8-11 and 13-15.

Accordingly, Applicants respectfully request that the rejection over claims 1-11 and 13-15 be withdrawn.

Other Matters

The specification has been amended to correct typographical errors that have come to Applicants' attention.

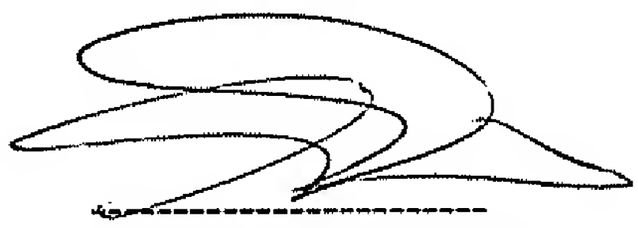
Added Claims

New claims 29-34 further define Applicants' invention and are believed to be patentably distinct from the applied art and in condition for allowance, as discussed above.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0458.

Respectfully submitted,
Huilong ZHU



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